



The Net Benefits of Single-Chip Integration for ZigBee SoC Solutions

When developing a 2.4 GHz ZigBee® wireless networking application, designers are often faced with a system partitioning choice: What is the optimal level of integration for a ZigBee connectivity and network processing solution? From a performance, power and cost perspective, what makes the most sense – a ZigBee system-on-chip (SoC) device that combines a 2.4 GHz wireless transceiver and a processing core into a single-chip solution or discrete approaches involving separate transceivers and host processors?

Before addressing these questions, let's take a closer look at ZigBee technology. Based on the IEEE 802.15.4 MAC/PHY specification for low-power wireless networks, ZigBee extends IEEE 802.15.4 by adding a mesh networking communications protocol and applications profiles that allow devices to fully interoperate. ZigBee uses a highly reliable, scalable mesh networking protocol that can support thousands of nodes. ZigBee applications profiles define a common language for home/commercial automation, smart energy, health care and retail devices. ZigBee also provides testing and certification of devices to ensure interoperability from the radio through the application layer.

ZigBee has been designed as a highly reliable, low-cost, low-power wireless networking solution for sensor and control networks. The choice of system partitioning ultimately has a significant impact on the network performance, power consumption and cost of a ZigBee solution.

System Partitioning

Figure 1 shows the three basic system partitioning options: the ZigBee SoC approach, a ZigBee network coprocessor (NCP) plus host processor, and ZigBee transceiver plus host processor.

In an SoC design, the IEEE 802.15.4 compliant radio is a peripheral to the embedded processor, and all of the packet processing and applications processing is performed within the single chip. The SoC typically includes hardware peripherals for the microprocessor to support computationally intensive functions such as AES encryption.

In an NCP design, the ZigBee stack operates on the radio and network processor chip, which is then connected to a host processor typically using a SPI or UART interface. The host is only active for those packets either sent or to be received by the application on that device. For packets that are routed, all packet processing including security processing, is done on the network processor without interrupting the host processor. The impact of SPI or UART processing time would therefore only be expected at the source or destination of a packet.

A ZigBee transceiver includes only the RF transceiver and the timing-critical MAC/PHY functions, while a host processor supports the upper layers of the MAC, network protocol and applications code. All packets must be moved to the host for processing. Those packets that are only to be routed are moved to the host and then back to the radio to retransmission, typically through a UART or SPI port. Often the AES

encryption operations are included on the transceiver chip; therefore, additional UART or SPI transfers are required to support the security processing.

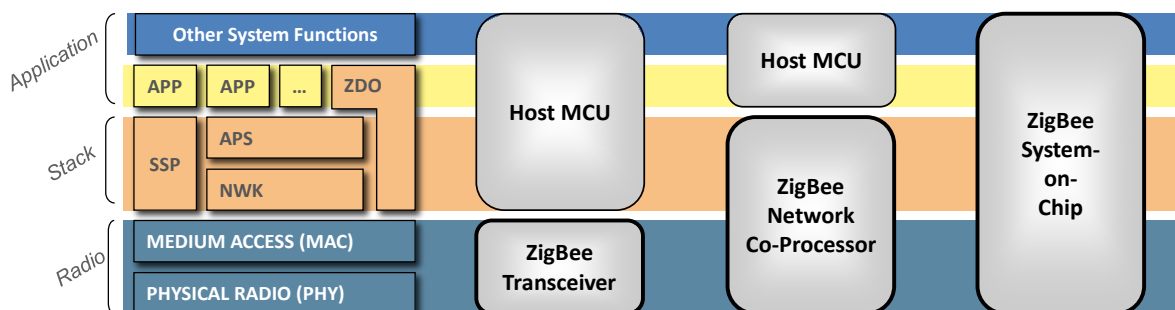


Figure 1. ZigBee System Partitioning Options

Network Performance

Throughput and latency should be considered in the system design to ensure the network will meet the design goals for the product. Throughput is a measure of how much data traffic the network can support and is a key metric because it determines the scalability of the network. Latency is a measure of how quickly messages are passed between nodes and is a key metric because it determines the responsiveness of the network. Throughput and latency are both a function of the device partitioning and must be considered in the system architecture.

ZigBee is a hybrid mesh networking protocol that includes a backbone of routers that are always active and end devices that are normally asleep. The routers are responsible for passing messages between the end devices or from end devices to a central controller. The throughput and latency of a ZigBee network is a function of how quickly routers can process data packets and forward them to the proper destination.

The efficiency of the routers is a function of the system partitioning. If the system uses an SoC or NCP, all of the routing is handled without needing to wake or interrupt the host processor. Packets are typically forwarded within 5-10 ms. If the system uses a transceiver, the transceiver needs to wake or interrupt the host processor to process each packet. The wake or interrupt latency can be >100 μ s. In addition, the packet data must be transferred between the transceiver and host processor. ZigBee packets can be up to 127 bytes (1016 bits), so transferring a packet to the host processor and back to the transceiver can take 0.5-4 ms at typical SPI/UART data rates. ZigBee uses AES encryption both at the MAC and network layers and sometimes even at the application layer. Additional UART or SPI data transfers will be required if either the host or the transceiver do not support efficient AES encryption.

Figure 2 shows the impact of system partitioning on network performance for a small 5-byte payload where AES encryption is only supported in the ZigBee transceiver. The latency of a single hop is 10 ms in a network that uses an SoC or NCP and 20 ms in a network that uses a transceiver. Since it takes each node twice as long to process a packet, the throughput of the network using transceivers has been reduced by 50 percent, which reduces the maximum number of devices that can be supported at a given activity level by 50 percent. For timing-sensitive applications such as lighting, the increased latency will limit the maximum number of hops allowed, reducing the scalability and reliability of the network.

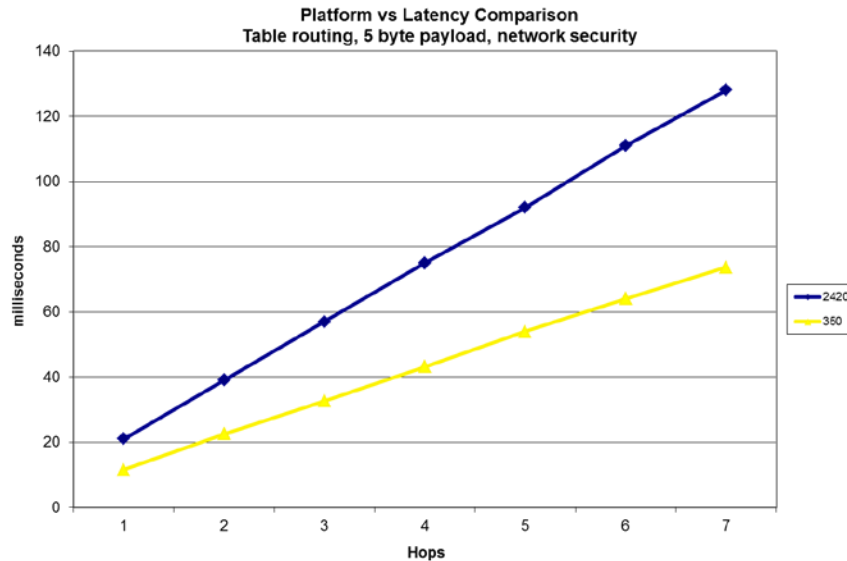


Figure 2. Latency versus System Partitioning

Power Consumption

The ZigBee communications protocol was designed to allow sleeping end devices to be in control of their battery life. Sleeping end devices set their own schedule for waking and interacting with the network to allow designers to determine the proper balance between battery life and data updates. In addition, the ZigBee protocol does not require any resynchronization of the sleeping end device when it wakes, so the data transfer to its parent is very efficient.

In a ZigBee network, the key power consumption metric is the battery life of the end nodes. A battery-powered end node is typically asleep and only wakes periodically to check if there is any data available from the network. When the battery-powered end device is asleep, the current consumption is dominated by leakage current.

During a data poll, the battery-powered end device must wake the processor, enable the transceiver, perform a clear channel assessment, transmit the data request, receive the acknowledgement and potentially receive data from the network. Most of these functions are performed at the MAC layer without interaction with the network stack. If the network has data for the end node, the time required to send the data from the router to the end node is a function of the system partitioning. If the router is an SoC or NCP, the data request can be processed internally, and the router typically responds within 2-3 ms. If the router uses a transceiver, the transceiver must wake or interrupt the host processor, wait for the processor to create the data packet and receive the data packet over the serial port, which can add up to 10 ms of delay. During this delay, the end node receiver must remain active, which can significantly reduce the battery life. This is unfortunate in that the device partition on the router has a negative impact on the battery life of the end device.

Cost Impact

The cost of a single-chip wireless SoC solution such as a Silicon Labs Ember® ZigBee® SoC or NCP is typically lower than a two-chip transceiver/host processor solution. The PCB cost is lower because less PCB area is required, there are fewer devices to assemble and less signals to route between devices.

The total cost of silicon is lower due to the elimination of redundant features such as AES hardware acceleration that are required at the MAC/PHY and network layers and the elimination of serial ports and pins used to communicate between the transceiver and the host. In systems where there is a large host processor, developers often consider it more cost-effective to add a transceiver to the design. However, in these systems, the impact on latency and throughput must be considered as part of this design choice.

Conclusion

For end devices and routers that do not require a host processor, the single-chip wireless SoC system partitioning approach delivers the best network performance, the lowest power consumption and the lowest overall cost. If a host processor is required by the system, the NCP system partitioning approach delivers the best performance and lowest power with the least impact on the host processor performance. Find out more about Silicon Labs' Ember® ZigBee platform at www.silabs.com/zigbee.

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